

REMARKS

Claims 1-60 are pending in the present application. In the Office Action, claims 1-5, 9-18, 22-31, and 35-39 were rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay, et al (U.S. Patent Application Publication No. 2003/0028633). The Examiner's rejections are respectfully traversed.

Lindsay describes Alert Standard Format watchdog timers 28 that are used to determine whether a device connected to a PCI bus is operating. If the device is operating, system BIOS in the device should continually reset the watchdog timer. In the event the devices not operating because of the loss of primary PCI bus power, it may be desirable to disable the watchdog timer so that the ASF firmware will not start the watchdog timer. See Lindsay, paragraph [0051]. However, Lindsay is completely silent with regard to a watchdog timer that is coupled to receive a reset input upon a predetermined change in a system state indicated by Alert Standard Format sensor data, as set forth in independent claims 1, 14, and 27.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Lindsay and request that the Examiner's rejections of claims 1-5, 9-18, 22-31, and 35-39 under 35 U.S.C. § 102(e) be withdrawn.

In the Office Action, the Examiner indicated that claims 6-8, 19-21, and 32-34 include allowable subject matter. Pursuant to the above discussion, Applicants respectfully submit that these claims are now in condition for allowance.

In the Office Action, claims 40-60 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Poisner (U.S. Patent No. 6,012,154) in view of Smit (U.S. Patent No. 6,393,589). The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

Poisner describes a watchdog timer 232 that may be used for detecting and/or recovering from computer system malfunctions. The watchdog timer 232 is located on an expansion bus

bridge 230 and may periodically receive a reset signal from a software agent 212 via a host bus 220. If the watchdog timer 232 expires, and interrupt signal may be asserted to a processor 205. See Poisner, col. 4, l. 66- col.5, l. 9 and Figure 2. However, as admitted by the Examiner, Poisner does not teach or suggest determining an expiration of a watchdog timer on an integrated circuit and responding to a system error by a microcontroller on the integrated circuit, as set forth in independent claims 40, 47, and 54. To the contrary, Poisner teaches that the watchdog timer 232 is deployed on the expansion bus bridge 230, which is a completely separate device from the processor 205 and a software agent storage area 210 that stores the software agent 212.


The Examiner therefore relies on Smit to describe a watchdog timer that is incorporated on the same chip as a microprocessor. The Examiner alleges that would have been obvious to make the proposed combination because Smit teaches that the integral watchdog timer provides improved flexibility to the system. However, Smit provides no particular suggestion or motivation for modifying the subject matter described in Poisner to arrive at Applicants claimed invention. Poisner also fails to provide any suggestion or motivation for modifying the prior art to arrive at Applicants claimed invention. To the contrary, Poisner describes a preferred embodiment in which the timer 232 is located in an expansion bus bridge 230. Accordingly, the prior art lacks any teaching that there is any particular advantage to incorporating the timer 232 described by Poisner on the same chip has a microprocessor.

For at least the aforementioned reasons, Applicants respectfully submits that the Examiner has failed to make a *prima facie* case that independent claims 40, 47, 54, and all claims depending therefrom are obvious over Poisner and Smit, either alone or in combination. Applicants request that the Examiner's rejections of claims 40-60 under 35 U.S.C. 102(b) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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